REMARKS/ARGUMENTS

The Office Action of May 29, 2008, has been carefully reviewed and these remarks are responsive thereto. Claims 1, 2, 8, 9, 19, 20, and 29-32., and 32 have been amended. Claims 1, 2, 8-10, and 16-32 are presently pending in this application. Claims 1, 2, 8-10, and 16-32 stand rejected. Applicant acknowledges withdrawal of the objections to the specification.

Reconsideration and allowance of the instant application are respectfully requested.

Claim Rejections - 35 U.S.C. §112

Claims 1, 2, 8, 9, and 16-19 are rejected under 35 U.S.C. 112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 2, 8, 9, and 16-19, the Office Action alleges (Page 2.):

> Above claims amend language qualifying the data as "state data" and subset of that as "data of interest". However neither claim nor specification defines "state data" and how a subset of that is selected to arrive at "data of interest".

Applicant believes that claims 1, 2, 8, 9, and 16-19 are in compliance with MPEP § 2171 because the claims set forth the subject matter that applicants regard as the invention and because the claims point out and distinctly define the metes and bounds of the subject matter. The claims include terms referring to "state data" and "data of interest," in which the specification is specific about these terms. For example, the specification discloses (Paragraph 28. Emphasis added.):

> As will be described in further detail, the debugging resource 122 receives and compacts state data from the emulation IC 120, and schedules the assignment of the state data to the pins 124. On-board bus 160, on-board trace memory 180, and reconfigurable interconnects 140 represent a broad range of buses, memory, and interconnects known in the art. Accordingly, these elements will not be described in detail below. **State data may include trace data, data of interest, ignored data,**

> **and other types of data**. Further, **data of interest may include all of the state data, a subset of the state data, and other types of data**.

The specification further discloses (Paragraph 36. Emphasis added.) :

> As illustrated in Figure 4A, the first select logic device 310 receives state data W 402. The first select logic device 310 comprises a data of interest sorter 440, for sorting state data. A data of interest sorter 440 may include a decoder and/or a controller. The controller may operate the decoder to sort the state data according to a predetermined operation, a consistent operation, or a changing operation. Further, **the data of interest sorter 440 may include a memory or an access to a memory that contains information regarding the location of data of interest bits in a sample of state data.** Data of interest sorter 440 may be software driven, hardware driven, or a combination of software and hardware driven.

As disclosed above, data of interest sorter 440 in conjunction with a memory may locate data of interest bits in a sample of state data. Figure 4A further provides embodiments in which state data 402, 404, 406, and 408 is processed by first select logic device 310 to obtain data of interest (*e.g.*, bits 450-452 and bits 481-484). (Paragraphs 37-39.) Applicant believes that claims 1, 2, 8, 9, and 16-19 are definite by particularly pointing out and distinctly claiming the subject matter which Applicant regards as the invention. Applicant requests reconsideration of claims 1, 2, 8, 9, and 16-19.

Claim Rejections - 35 U.S.C. §103

Claims 1, 2, 8-10, and 16-32 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent Publication No. 2002/0065642 (Swoboda) in view of U.S. Patent No. 6,816,989 (Litt) further in view of U.S. Patent No. 6,092,127 (Tausheck).

Regarding claim 1, Applicant is amending the claim to include some of the features from dependent claim 8 and the feature of "selecting a second data of interest from the second sample of state data, wherein the second data of interest is a second subset of bits of the second sample of state data and **wherein bit locations of the first data of interest and the second data of interest are**

different." (Emphasis added.) The amendment is supported by the patent application as originally filed, *e.g.,* Figure 4A and Paragraphs 36-39.

The Office Action alleges that (Page 7.):

> Swoboda teaches a method in an emulation system (Swoboda: Fig.2 & associated disclosure), comprising receiving a first sample of state data (Swoboda: Fig.9 & and associated disclosure); selecting data of interest from the first sample of state data (Swoboda: Fig.9 state data having at least Data, Address, PC"), wherein the data of interest is a subset of bits of first sample of state data and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest (Swoboda: Fig.19 & [0121]). Further Swoboda teaches storing the data for transmission such that first and second portions of the data of interest are no longer separated by at least a bit as selecting the data of interest from the packet (Swoboda: Fig.19 & [0121], See Data Bvte 1 and Data Bvte 2) and then aligning them for transmission (Swoboda: [0122]-[128], [130] & Fig.2, 8, 21, 22 and 23, 23 A-B).

Swoboda merely discusses a compression map as shown in fig. 19 in order to process selected data (*i.e.,* data of interest) (data byte 1, data byte 2, and data byte 5) from packet 91 as shown in fig. 9. (Paragraph 121.) However, Swoboda fails to discuss any thing about the location of selected data being different when processing different packets. Moreover, Litt and Tausheck fail to remedy the deficiencies of Swoboda. Litt merely discusses a bandwidth manager for assisting in the offloading of internal state data (column 3, lines 28-42) while Tausheck merely discusses chained direct memory access operations (column 2, lines 20-46).

Applicant is similarly amending independent claim 20 to include the feature of "a first select logic device configured to receive samples of state data, to select data of interest from each of the samples of state data, the data of interest having non-contiguous bits, and to sort the data of interest such that the non-contiguous bits become contiguous, wherein selected bit locations of the data of interest from at least two samples are different." The Office Action alleges that (Page 11.):

> Litt teaches an apparatus having a first select logic device configured to receive samples of state data, to sort samples of state data, and to select data of interest from each of the samples of state data (Litt: Fig.2, Elements 210 & 215, Col.6 Lines 3-34); first and second buffers coupled to the first select logic device and configured to receive the selected data of interest (Litt: Fig.2 Elements 225a 225b); a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer (Litt: Fig.2 Elements 250); and an output storage device coupled to the second select logic device and configured to receive data drained from the selected buffer (Litt: Fig.1 Element 50).

However, Litt merely discusses bandwidth manager 125 that selects data from two or more data streams within an integrated circuit, where the incoming data sources represent state data from regions within the integrated circuit. The selection of the incoming data stream is determined by signal VP (as shown in fig. 2 but not numbered), which may be based on a configuration and status register. (Column 8, lines 34-48.) However, Litt is silent about selecting data from samples of state data in which the bit locations are different, and thus does not teach the feature of "a first select logic device configured to receive samples of state data, to select data of interest from each of the samples of state data, the data of interest having non-contiguous bits, and to sort the data of interest such that the non-contiguous bits become contiguous; wherein selected bit locations of the data of interest from at least two samples are different."

Regarding independent claim 29, Applicant is amending the claim to include the feature of "determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of plurality of pins is shared by at least two trace data chains." The amendment is supported by the patent application as originally filed, *e.g.,* Figures 7 and 8A-8C and Paragraphs 34

and 57- 58[1]. (For example, trace chain C1 710 has access to trace pin P1 855 during the first clock cycle and trace chain C3 730 has access to trace pin P1 855 during the second clock cycle.)

> The Office Action admits that (Page 14.):
>
> Litt does not teach a pin manager explicitly that would perform the steps of offloading the data. Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [128]).

However, as shown in fig. 22, Swoboda merely discusses pin manager 224, which routes a single stream of transmission packets to desired pins of a debug port[2]. (Paragraph 128.) However, Swoboda is silent about routing a plurality of packet streams and thus fails to even suggest the feature of "determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of the plurality of pins is shared by at least two trace data chains."

Applicant is similarly amending independent claim 30 to include the feature of "associating a set of the plurality of trace data chains with the plurality of pins in accordance with the determined

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[1] The present specification discloses trace chain 300, where storage device 340 is capable of sequentially outputting data, *i.e.,* outputting a data stream. (Paragraph 34.) Trace pin select logic 770 receives data streams from a plurality of trace chains (710 to 780). (Paragraph 57.) Also, trace chain C1 710 has access to trace pin P1 855 during the first clock cycle and trace chain C3 730 has access to trace pin P1 855 during the second clock cycle. (Paragraph 58.)

[2] Swoboda recites "FIG. 22 illustrates pertinent portions of exemplary embodiments of the trace export portion of FIG. 2. As shown in FIG. 22, the trace export portion includes a FIFO buffer coupled to a transmission formatter 220. The FIFO buffer receives the composite trace stream produced by the stream combiner 85 (see also FIG. 8). **The transmission formatter 220 outputs a stream of transmission packets to a pin manager 224 which routes the packets to desired pins of, for example, a debug port on the target chip**. Continuing with the above-described 10-bit trace packet example, the stream combiner 85 produces a composite stream of 10-bit trace packets. The trace export portion, including the FIFO buffer and transmission formatter 220, transforms the trace packets of the composite packet stream into a stream of transmission packets that can have a different bit width than the 10-bit trace packets. This stream of transmission packets is sent sequentially from the pin boundary of the target chip to the trace recorder of FIG. 2. The transmission packets can be delivered to the trace recorder via, for example, the debug port or another system bus port.' (Paragraph 128. Emphasis added.)

schedule, wherein one of the plurality of pins is shared by at least two trace data chains." Claim 31, as amended, includes the similar feature of "a memory coupled to the trace pin select logic device and configured to store a schedule to associate the selected set with the pins based at least upon determined trace data chain fill rates of the set, wherein one of the plurality of pins is shared by at least two trace data chains."

Applicant requests reconsideration of claims 1, 2, 8-10, 16-28, and 32. Dependent claims 2, 8-10, 16-19, 21-28, and 32 are patentable over Swoboda in view of Litt and in further view of Taushek, taken alone or in combination, at least on the basis of their dependency from their respective base claims, and further in view of the additional features recited therein. Applicant does not concede the correctness of the Office Action's rejection with respect to any of the dependent claims discussed above. Accordingly, Applicant reserves the right to make additional arguments as may be necessary to further distinguish the dependent claims from the cited references, taken alone or in combination, based on additional features contained in the dependent claims that were not discussed above.

CONCLUSION

All issues having been addressed, Applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the Examiner is requested to contact the undersigned. Applicant respectfully requests further examination on the merits of this application.

Respectfully submitted,

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